ABSTRACT OF THE DISCLOSURE

The present invention, generally speaking, takes advantage of the foregoing capability to determine and display the X,Y location corresponding to a net name, by translating functional test data of a digital logic chip passed through a simulation model which identifies one or more defective nets of the chip. The defective nets are processed against a database of the foregoing type to obtain X,Y coordinate data for these nets, allowing them to be data logged as physical traces on the chip layout. In accordance with an exemplary embodiment, this mapping is performed by taking the output from a functional tester and translating it from a list of failed scan chains into a list of suspected netlist nodes. The X,Y coordinates of suspected netlist nodes are then identified and stored in a database, providing failure analysis and yield enhancement engineers a starting point for performing failure analysis and for immediately understanding whether "in-line" inspection data can account for a given failure. These nodes may then be crossmapped from the circuit design onto the chip's layout for each of multiple photomask layers within the design. Detailed failure data is gathered and stored at the wafer stage as part of a comprehensive program rather than on an as-needed basis at the packaged part stage. A voluminous amount of high-quality data is therefore obtained in an entirely automated fashion, as opposed to obtaining a comparatively minuscule amount of lesser-quality data in an exceedingly laborious fashion.